IN THE SPECIFICATION:

Replace the paragraph bridging page 10, line 19 through line 3 in page 11, as follows:

-- The above steps can be understood easily by the illustration shown in FIG 3. Upon a reception of the signal S identical to the signal F, the A-law codec 320 demodulates one channel of the A-law modulated signal F selected by the channel select signal S_[[SF]] FS into an analog signal. The demodulated analog signal is then applied to the μ-law codec 310 which in turn modulates the analog signal to generate the μ-law modulated digital signal P which is identical to the signal E of FIG. 2. --

BSH 5/30/07

Replace the paragraph ~~bridging~~ page 10, line 19 through line 3 in page 11, as follows:

-- In the meantime, the channel select signal S_FS is supplied to the first mixer 214 as a mixing control signal J. For the duration of the signal J (i.e., 3.9μsec), the first mixer 214 blocks an output path of the second buffer 214b of the first mixer 214 from transmitting the buffered B signal, and connects an output path of the first buffer 214a of the first mixer 214 for the transmission of the signal E. Thus, for the duration of the channel select signal S_FS (3.9μsec), the first mixer 214 selectively outputs the signal E while cutting off the signal B received thereon. Accordingly, if the signal B comprises 32 channels, only one channel selected in response to the channel select signal S_ [[FX]]

FS, is modulated by μ-law coding, and the remaining 31 unselected channels are output to the first mixer 214 without any conversion operated thereon by the codec 210.

BSH 5/30/07

Replace the paragraph ~~bridging~~ page 12, line 10 through line 15 in page 12, as follows:

More detailed functions of the codec 210 is further described by following the features shown in FIG 3. Upon reception of the signal R identical to the signal G, the μ-law codec 310 demodulates the selected channel of the μ-law modulated signal R (or G) in response to the channel select signal S_ [[SF]]FS into an analog signal. The demodulated analog signal is supplied to the A-law codec 320, in turn the A-law modulates the analog signal into the A-law modulated signal Q, which is identical to the signal H of FIG. 2.

IN THE SPECIFICATION:

BSH 5/30/07

Replace the paragraph starting at page 7, line 13 as follows:

Referring to FIG. 2, the codec apparatus includes a codec 210, a channel selector 212 for generating a channel select signal, S_FS and a first mixer 214 and a second mixer 216. The channel selector 212 outputs the channel select signal S_FS and mixing control signals J and K, which are controlled by a clock signal CLKx, a frame sync signal FSx, an read address, and data input. One skilled in art would know that ~~that~~ there are various ways and type of circuits served to provide an address generator controlled by a clock signal from a clock domain, which can generate read address for reading out data from the data storage elements. The codec 210 has input/output terminals for receiving and supplying the A-law modulated digital signals B and D, respectively, and input/output terminals for receiving and supplying the Φ-law modulated digital signals A and C, respectively. The codec 210 selectively converts a specified channel signal from the modulated multi channel signals in response to the channel select signal, S_FS generated by the channel selector 212. The first mixer 214 includes two buffers operating complementarily to each other in response to the mixing control signal J, a first buffer 214a for storing the digital signal output E from the codec 210 and a second buffer 214b for storing the original digital signal B. Similarly, the second mixer 216 consists of two